CLAIM AMENDMENTS:

Please amend Claim 17 as follows:

1.-16. (Canceled)

17. (Currently Amended) A memory controller comprising:

a converter section adapted to perform serial/parallel conversion of input image data of "a" bit width into image data of "a" x "2n"-bit width, where "a" is a natural number representing a size of the inputted bit width and "n" is a natural number;

a first FIFO (first-in-first-out) section adapted to temporarily store the image data of"a" x "2n"-bit width;

a frame memory section adapted to store image data of one frame; and

a second FIFO section adapted to temporarily store image data read out from said frame memory section,

wherein the image data is read out from said first FIFO section at the time of completion of storage of the image data therein, written into said frame memory section at half of a rate at which the image data is inputted into said converter section, and read out from said frame memory section[[,]] at a rate that is half of a rate at which the image data is inputted into said first FIFO section, ~~and,~~

wherein the time period for writing into the frame memory section is less than the time period during which the image data is stored in the first FIFO section, and in

which the writing in and reading out of image data to and from the frame memory section is effected through a single input/output terminal,

wherein said first FIFO section is of a size suitable for storing image data, so that, within a period for inputting the image data into said first FIFO section to FULL capacity, writing the image data into said frame memory section, reading the image data from said frame memory section, and executing a command of said frame memory section are conducted, and wherein

successive frames of image data are successively written.

18. (Previously Presented) A liquid crystal display comprising:

a liquid crystal panel;

a decoder adapted to convert an inputted image signal into an image signal adaptable to said liquid crystal panel,

wherein said decoder is provided with a memory controller according to Claim 17.